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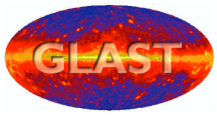	**LAT-SS-00363-04**	10/303/02
	Prepared by(s) M. Amato, G. Shiblie G. Haller, M. Nordby, G. Unger, D Shepard, K. Segal	Supersedes Previous
GLAST LAT SUBSYSTEM SPECIFICATION	Subsystem/Office ACD Subsystem, Electrical and Mechanical systems	
Document Title **ACD-LAT Interface Control Document (ICD) – Mechanical, Thermal and Electrical**		

Gamma-ray Large Area Space Telescope (GLAST)

Large Area Telescope (LAT)

ACD-LAT Interface Control Document (ICD) – Mechanical, Thermal and Electrical

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CHANGE HISTORY LOG

Revision	Effective Date	Description of Changes
1	12/28/01	Initial Draft
2	4/4/02	Initial Release – Authorized
3	4/29/02	Draft of combined version of Mech and Elect ICD

Table of Contents

List of Figures

1. Purpose

One purpose of this document is to establish the electrical interface between the ACD Front-end Electronics (i.e. Front-end event electronics (FREE) circuit card) and the ACD Electronics Module (AEM). The second purpose of this document is to establish and describe the mechanical and thermal interfaces to and from the Anticoincidence Detector (ACD) subsystem of the LAT. It is intended to be used to delineate interfaces, so subsystems components can be designed and fabricated based on clear, understood values for their interfaces to the rest of the LAT. This ICD will also serve as a requirements list against which interface tests are developed, and against which the ACD subsystem must be verified prior to integration on the LAT.

2. Scope

The scope of this ICD document includes two areas. One is the electrical interface between the ACD Front-end Electronics (i.e. Front-end event board) and the ACD Electronics Module. The interconnections as well as the commanding and dataflow are described. The second area includes all mechanical and thermal interfaces between the LAT and the ACD. This document also covers the physical routing of cables, cable size, support, stay-clears and heat generated by electronics.

3. Acronyms

ACD – Anticoincidence Detector

ADC – Analog to Digital Converter

AEM – ACD Electronics Module

AGN – Active Galactic Nuclei

BEA – Base Electronics Assembly

BOL – Beginning of Life

CAL – Calorimeter

CFC - Carbon Fiber Composite

CG – Center of Gravity

CNO – Carbon-Nitrogen-Oxide

CTE - Coefficient of Thermal Expansion

DC – Direct Current

DFS – Data-Flow System

EMI – Electromagnetic Interference

EOL – End of Life

FREE – Front-End Electronics

GAFE – GLAST Analog Front End

GARC – GLAST Analog Readout Controller

GLAST – Gamma-ray Large Area Space Telescope

GLT – Global Trigger

GRB – Gamma-Ray Burst

GSE - Ground Support Equipment

GSFC – Goddard Space Flight Center

HLD – High Level Discriminator

HVBS – High Voltage Bias Supply

ICD – Interface Control Document

IRD – Interface Requirements Document

LAT – Large Area Telescope

LLD – Low Level Discriminator

LVDS – Low Voltage Differential Signal

M-GSE - Mechanical Ground Support Equipment

MIP – Minimum Ionizing Particle

MLI – Multi-Layer Insulation

MPLS – Multi-Purpose Lifting Sling

MSB – Most Significant Bit

N – Newtons

PMT – Photo-Multiplier Tube

RMS – Root Mean Square

SRD – Science Requirements Document

TACK – Trigger Acknowledge

TBR – To Be Resolved

TBD - To Be Determined

T&DF – Trigger and Dataflow System

TEM - Tower Electronics Module

TKR – Tracker

TRG – Trigger

TSA – Tile Shell Assembly

4. Definitions

sec, s – Microsecond, 10^{-6} second

Analysis – A quantitative evaluation of a complete system and /or subsystems by review/analysis of collected data.

Background Rejection – The ability of the instrument to distinguish gamma rays from charged particles.

cm – centimeter

Cosmic Ray Œ Ionized atomic particles originating from space and ranging from a single proton up to an iron nucleus and beyond.

Demonstration – To prove or show, usually without measurement of instrumentation, that the project/product complies with requirements by observation of results.

Event – an event results in that the instrument is triggered and the data associated to that event is read out.

Inspection – To examine visually or use simple physical measurement techniques to verify conformance to specified requirements.

Nominal MIP – 1 MIP produces a PMT anode signal of 0.64pC

MeV – Million Electron Volts, 10^6 eV

MHz – Megahertz, 10^6 hertz

s, sec – seconds

Simulation – To examine through model analysis or modeling techniques to verify conformance to specified requirements

TACK - Trigger Acknowledge signal distributed from the trigger system to the detector sub-systems. The sub-systems save the event data in an event buffer when receiving this signal.

Testing – A measurement to prove or show, usually with precision measurements or instrumentation, that the project/product complies with requirements.

Trigger – generates a decision whether to readout the instrument and distributes a Trigger Acknowledge to acquire event data considering data received from the detector sub-systems.

V - Volts

Validation – Process used to assure the requirement set is complete and consistent, and that each requirement is achievable.

Verification – Process used to ensure that the selected solutions meet specified requirements and properly integrate with interfacing products.

5. Applicable Documents

1. LAT-SS-00458 LAT Electronics Subsystem Preliminary Design Report
2. LAT-SS-00289 Conceptual Design of the LAT ACD Electronics Module
3. LAT-SS-00291 Electrical Grounding and Shielding Plan
4. GSFC-433-RQMT GLAST EMI/EMC Requirements Document
5. Directive 561-PG-8700.2.1, Flight FPGA Design Guidelines
6. Directive 564-PG-8700.2.1, Microelectronics and Signal Processing Branch
7. LVDS Owner's Manual (A General Design Guide for National's LVDS and Bus LVDS Products), 2nd Edition
8. LAT-DS-00038 LAT Mechanical Systems Mechanical Integration LAT Instrument Layout
9. LAT-DS-00309 LAT Mechanical Systems Interface Definition Dwg
10. GEVS-SE General Environmental Verification Specification for STS & ELV Payloads, Subsystems, and Components
11. LAT-SS-00016 ACD level III requirements/specifications
12. LAT-SS-00352 ACD level IV requirements/specifications
13. LAT-SS-00010 LAT level IIb specifications
14. LAT-TD-00778 LAT Environmental ~~Test Parameters~~Specification
15. LAT-TD-00890 LAT Instrumentation Plan
16. LAT-DS-TBD ACD Outline Drawing
17. ANSI Y 14.5M

6. Mechanical Interface Description

6.1.General Description

The ACD interfaces with the LAT in three ways. First, the support off the Grid provides primary structural and thermal interface to the remainder of the LAT. This provides the structural support and stability for the ACD, as well as the primary means for conductive heat transfer. The second interface is the radiative thermal coupling to the outer space environment, through the MLI surrounding the ACD. The final interface is the radiative thermal interface between the ACD inside surface and the TKR modules and Grid.

These three interfaces are described in detail, and requirements for both sides of the interfaces are specified in this document. The reference coordinate system is shown in LAT-ACD Interface Definition Drawing (IDD), LAT-DS-00309, and the System of Units used shall be metric. Any drawings included in this document or referred to shall meet ANSI Y14.5M standards.

Mass Properties -Mass shall be less than 235 Kg (approved Feb 2002), The CG shall be under 393 mm in the Z axis and +/- 5mm in the x and y axis

6.2.ACD Responsibilities

6.2.1.Flight Hardware

Development, fabrication, test, and delivery of the following components:

ACD flight unit with interfaces as described in this document.

MLI and micrometeoroid shield to cover the ACD, with thermal properties and coverage as defined in this document. The exact interface of the ACD MLI to the rest of the LAT MLI is still TBD.

Bolts, washers, and any other hardware needed to attach the ACD to the Grid.

Thermally conductive material, as needed to meet the interface requirements described below, to be used at the ACD-Grid interface joint.

6.2.2.Flight GSE

Development, fabrication, test, and delivery of the following mechanical ground support equipment (M-GSE):

Lifting harnesses, shackles, and any other temporary hardware needed to support the ACD during integration on the LAT.

Handling Dolly to the support and move the ACD prior to integration to the LAT.

Any needed drill templates/pin templates.

Micrometeoroid shield/thermal blanket removal tools if needed.

ACD multi purpose test fixture.

Hydraset capable of manipulating ACD if needed.

6.3.LAT Responsibilities

6.3.1.Flight Hardware

Development, fabrication, and test of the following components:

Grid structure to support the ACD, with interfaces as specified in this document.

The ACD to LAT AEM flight cable harness.

Cableway and attachments for routing of the ACD to LAT AEM cable harness to the LAT AEM boxes under the LAT.

LAT is responsible for the flight cables coming from the connectors on the ACD BEA.

Flight GSE

Development, fabrication, and test of the following components:

Crane for lifting the ACD with its lifting fixture. Capacity ->235 Kg.

Lifting fixture for the ACD, which meets the requirements of Section 13.3.

~~7.~~6. ~~Structural~~ Mechanical Interfaces ~~Interface~~

6.1. General Description

The ACD-Grid interface is the primary mechanical interface for the ACD. This provides the structural support and stability for the ACD, and provides a stable reference by which the ACD position is surveyed and maintained. This interface also provides the primary means for conductive heat transfer.

These three interfaces are described in detail, and requirements for both sides of the interfaces are specified in this document.

The reference coordinate system is shown in LAT Coordinate System, LAT-TD-00035.

The System of Units used shall be metric.

The most up to date Grid drawing and the most up to date versions of other drawings referred to in this document reside on the LAT web site on Cyberdocs.

All drawings included in this document or referred to shall meet ANSI Y14.5M standards.

6.2. Flight Hardware

6.2.1. ACD Responsibilities

Development, fabrication, test, and delivery of the following components:

ACD flight unit with interfaces as described in this document.

MLI and micrometeoroid shield to cover the ACD, with thermal properties and coverage as defined in this document. The exact interface of the ACD MLI to the rest of the LAT MLI is still TBD.

Bolts, washers, and any other hardware needed to attach the ACD to the Grid.

Thermally conductive material, as needed to meet the interface requirements described in this document, to be used at the ACD-Grid interface joint.

6.2.2. LAT Responsibilities

Development, fabrication, and test of the following components:

Grid structure to support the ACD, with interfaces as specified in this document.

The ACD to LAT AEM flight cable harness.

Cableway and attachments for routing of the ACD to LAT AEM cable harness.

6.3. Mass Properties

6.3.1. Mass

The ACD mass will be less than 235 Kg (approved Feb 2002).

6.3.2. Center of Gravity

The CG will be under 393 mm in the Z axis and 0 +/- 5mm in the X and Y axis.

~~7.1.~~6.4. Structural Mounting and Load Transfer

~~7.1.1.~~6.4.1. ACD Requirements

~~The ACD mounts to the Grid. The most up to date Grid drawing and the most up to date versions of other drawings referred to in this document reside on the LAT web site on Cyberdocs.~~ The ACD is mounted to the Grid as shown in the LAT-ACD IDD drawing, LAT-DS-00309.

–The ACD mount to the Grid shall conform to the dimensions and tolerances shown in LAT-ACD IDD drawing, LAT-DS-00309.

–There is currently no specific requirement for surface preparation or coefficient of friction; friction will not be assumed to carry any load.

The ACD structure at the Grid interface shall have a CTE of 21-25 x 10^{-6} m/m/degC (consistent with aluminum material)

~~7.1.2.~~6.4.2. LAT Requirements

The Grid mounting bosses for the ACD shall conform to the dimensions and tolerances shown in LAT-ACD IDD, ~~drawing (~~LAT-DS-00309~~)~~.

The Grid structure shall have a CTE of 21-25 x 10^{-6} m/m/degC (consistent with aluminum material)

The Grid must be available for Grid to ACD pinning operation and fit check; this will be done during fit check before delivery.

~~7.2.~~6.5. Structural Interface Loads

Maximum expected reactions at the LAT-ACD interface are listed in Table 1. These reactions are the latest results from the coupled loads analysis released July 2002.

Table 1 Design Loads for the ACD BEA Interface to the Grid (TBR)

Load Case:	lat8al(2+3)1			lat8al(2+3+4)			lat8al(2+3)2		
Mount Location	**Fx (N)**	**Fy (N)**	**Fz (N)**	**Fx (N)**	**Fy (N)**	**Fz (N)**	**Fx (N)**	**Fy (N)**	**Fz (N)**
-X/-Y Corner (Bay 0)	0	0	-1011	0	0	-1275	0	0	-183
+X/-Y Corner (Bay 3)	0	0	832	0	0	27	0	0	-113
-X/+Y Corner (Bay 12)	0	0	-1011	0	0	-206	0	0	-184
+X/+Y Corner (Bay 15)	0	0	833	0	0	1097	0	0	-112
Lower +X Mid-side	-394	0	-676	-445	-2064	-855	-938	0	-2120
Upper +X Mid-side	-294	0	-166	-10	-1400	-384	1086	0	-1475
Lower -X Mid-side	746	0	-1910	695	-2064	-1731	952	0	-2169
Upper -X Mid-side	-1649	0	-1648	-1365	-1400	-1431	-1162	0	-1534
Lower +Y Mid-side	-2979	-572	-1281	-2106	-403	-734	-117	-948	-2123
Upper +Y Mid-side	-1933	680	-928	-1367	-60	-289	-76	1127	-1541
Lower -Y Mid-side	-2979	571	-1278	-2107	740	-1825	-117	948	-2123
Upper -Y Mid-side	-1932	-679	-931	-1366	-1419	-1569	-75	-1127	-1541

Corner Mount Design Loads		**Mid-side Mount Design Loads**	
Pull-out (N)	1097 / -1275	**Pull-out (N)**	1127 / -1649
Shear (N)	0	**Shear (N)**	3242.746059

Notes:

ACD BEA to Grid Joint:

- Bolted connection at four corners of BEA carry z-direction (thrust) loads only
- Bolted and pinned connections at the center of each of the 4 sides
- Interface loads evaluated by retrieving nodal forces at rigid extension from Grid to BEA.

~~7.2.1.~~6.5.1. ACD Requirements

The ACD shall be able to withstand launch loads, as specified in LAT requirements and in LAT Instrument-Spacecraft IRD (433-IRD-0001).

ACD interfaces with LAT shall be able to withstand the maximum expected interface reactions without any violation of the ACD structural requirements. This will be demonstrated by test and/or analysis. ~~Note that the maximum reactions listed in Table 1 may be exceeded in some locations during strength qualification testing. This possibility should be taken into consideration during design. If future updated LAT structural analyses produce reactions lower than the maximums listed in Table 1, then those lower reactions shall be used to size the ACD interfaces to LAT.~~

~~7.2.2.~~6.5.2. LAT Requirements

The Grid shall be capable of tolerating the reaction forces due to ACD acceleration and vibration loading. LAT interfaces with ACD shall be able to withstand the maximum expected interface reactions without any violation of the LAT structural requirements. This will be demonstrated by

test and/or analysis. ~~Note that exceedances of the maximum reactions listed in Table 7.2.1 is possible during strength qualification testing and should be taken into consideration during design. If future updated LAT structural analyses produce reactions lower than the maximums listed in Table 1, then those lower reactions shall be used to size the LAT interfaces to ACD.~~

~~7.3.~~6.6. Mechanical ~~testing~~Testing

~~7.3.1.~~6.6.1. ACD Requirements

The ACD shall be able to withstand the component-level random vibration levels and sine sweep levels shown in LAT Instrument-Spacecraft IRD (433-IRD-0001), with levels corrected for unit mass.

The ACD shall be able to withstand the acoustic levels shown in LAT Instrument-Spacecraft IRD (433-IRD-0001).

The ACD shall be capable of normal operation after the application of the external shock levels given in LAT Instrument-Spacecraft IRD (433-IRD-0001).

Mechanical environmental tests are also specified in LAT-MD-00408, LAT Program Instrument Performance and LAT-TD-00430, ACD I&T plan.

Instrumentation (accelerometers and strain gauges) needed for test are defined in LAT-TD-00890, LAT Instrumentation Plan.

~~7.3.2.~~6.6.2. LAT Requirements

The Grid shall be capable of tolerating the reaction forces due to ACD acceleration loading.

The Grid shall be capable of tolerating the reaction forces due to ACD vibration loading.

LAT will provide enough information for ACD to manufacture a Grid simulator for testing purposes.

~~8.~~7. Dimensions

Stay-clear dimensions are not-to-exceed dimensions. The nominal dimensions plus any needed tolerances ~~should~~ will be included within this stay-clear. These dimensions are defined, and will be measured with respect to a unique datum reference system.

~~8.1.~~7.1. Nominal Stay-Clear Dimensions

The ACD subsystem components shall stay within the stay-clear volume described in LAT-ACD IDD drawing, LAT-DS-00309. ACD stay-clears and dimensions shall be quoted and measured with respect to the datum reference system defined in the LAT-ACD IDD drawing, LAT-DS-00309 ~~, unless explicitly defined otherwise.~~ Stay-clear dimensions are to be measured at 21 +/- 3 degrees C.

~~The ACD subsystem components shall stay within the stay-clear volume described in LAT-ACD IDD drawing, LAT-DS-00309.~~

~~8.2.~~7.2. Stay-Clear for Dynamic and Thermal Motions

Maximum excursions beyond the static stay-clears are:

Allowed Lateral Dynamic Motions

1 mm inward motion of the TSA CFC shell.
2 mm outward motion of the TSA CFC shell on the outside of the ACD.
10 mm outward motion of the MLI shielding.
Thermal contraction/dilation of the interfaces to the Grid, consistent with the thermal expansion coefficient of aluminum.

Allowed Vertical Dynamic Motions

4 mm downward motion of the TSA CFC shell.

~~9.~~8. ~~General Electrical Interface Description~~Electrical Interfaces

The AEM electrically interfaces to the ACD Electronics at the 24 connectors located around the ACD Base Electronics Assembly (BEA) as shown in Figure ~~Figure Figure~~ 1. The ACD electronics harness connects the 12 ACD front-end electronics (FREE) circuit cards through the LAT DAQ EMI shield to the primary (A) and secondary (B) AEMs. Twenty-four (24) bulkhead connectors penetrate the LAT DAQ EMI shield. The cables that route from the AEMs to the LAT DAQ EMI shield are internal to the LAT and shall not be defined in this document. The harness connecting the ACD front-end to the LAT EMI shield connectors is described in this document. The LAT DAQ subsystem is responsible for all cables between the Base Electronics Assembly and the LAT DAQ EMI shield and between the LAT DAQ EMI shield and AEMs.

All signal characteristics are specified and measured on connectors at the BEA interface.

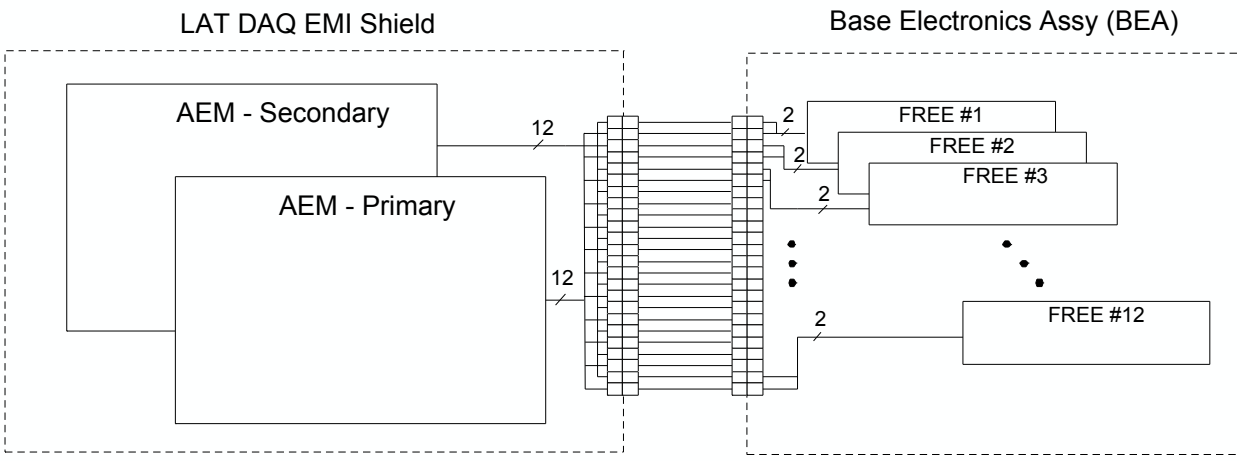


Figure 1. AEM to ACD Electrical Interface

~~9.1.~~8.1. ACD to LAT Electrical Interfaces

The ACD electrically interfaces to three LAT Instrument subsystems. The ACD electronics interfaces to the AEM through 24 connectors (twelve to A AEM and twelve to B AEM) that are mounted on the BEA. These connectors carry all of the ACD digital I/O signals and power to ACD; and some of the analog sensors. All of the temperatures sensors that are distributed on the ACD outside of the BEA electrically interface to both the LAT Power Distribution Unit (PDU) and to the Spacecraft Interface Unit (TBR).

~~9.2.~~8.2. Cable and Connectors Between ACD and LAT

~~9.2.1.~~8.2.1. ACD BEA and LAT EMI Skirt

~~9.2.1.1.~~8.2.1.1. ACD Base Electronics Assembly Bulkhead Connector, (Receptacle)

The connector part number is D38999/20FG-35-P which is a MIL-DTL-38999 Series III Scoop-Proof, 3 Way Self-Locking, Threaded Coupling metal shell connector with size 22 (high-density) contacts. The shell size is 21, and number of pins is 79. The arrangement of pins is shown below. Figure ~~Figure Figure 2~~ shows the connector.

This connector is listed on the NASA Parts Selection List (NPSL) and data may also be found at the following website, http://nepp.nasa.gov/npsl/Connectors/m38999/38999_s3.htm. The ACD bulkhead connectors have male pins.

Twelve (12) of the 24 total connectors interface to the A AEM connectors, and the other 12 connectors interface to the B AEM connectors. There are 60 conductors for each cable and interface and the signal are identified in Table 3, Signals List.

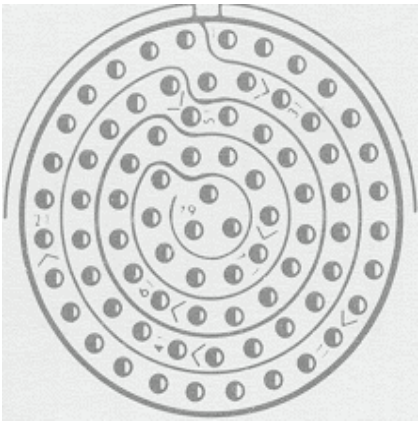


Figure 2. E35 Pin Arrangement

~~9.2.1.2.~~8.2.1.2. Connector at ACD BEA Side, (Plug)

This connector is a plug that mates to the bulkhead connector listed in8.2.1.1~~8.2.1.19.2.1.1~~. The connector part number is D38999/26FG-35-S which is a MIL-DTL-38999 Series III Scoop-Proof, 3 Way Self-Locking, Threaded Coupling metal shell connector with size 22 (high-density) contacts. The shell size is 21, and number of pins is 79. The arrangement of pins is shown in Figure 2. This connector shall have a right-angled backshell selected from the NPSL for cable strain relief, part number M85049/76-20xxx.

This connector is listed on the NASA Parts Selection List (NPSL) and may be found at http://nepp.nasa.gov/npsl/Connectors/m38999/38999_s3.htm. This connector has sockets.

~~9.2.1.3.~~8.2.1.3.Connector at ACD Electronics Module Side (for info only)

The connector on the AEM is a right angle 100 pin micro-D metal shell connector manufactured by Cristek Interconnects, Inc. The part number is MCR-1-100-1B1.

~~9.2.1.4.~~8.2.1.4. Harness between ACD BEA and ACD Electronics Module

The harness from the ACD BEA to the LAT EMI shield is approximately 0.75 m long (Ref) and consists of 24 AWG wires for all signals and power. The power lines in the harness will have a harness shield, separate from the harness shield on the signal wires. These shields shall be grounded at both ends. The overall harness shall also have a harness shield, which shall be grounded at both ends. The method used to ground these shields shall provide optimum grounding

contact with the backshell and connector and should avoid using a drain wire for grounding the shield.

The harness from the LAT EMI shield to the AEM has the same design, and is up to 1 m (Ref) long.

~~9.2.1.5.~~8.2.1.5. Naming Convention for Connector Designators

The following Table 2 lists the designation for each connector at the BEA interface. The connectors mounted on the BEA shall be clearly marked with these designations. The mating connectors at the end of the DAQ cables shall be clearly labeled with these designations.

Table 2. Connector Reference Designator

FREE Designator	ACD Location	Connecting AEM	BEA Connector Designator	LAT Cable Designator	LAT Cable Number
1LA	+Y, Left	Prime(A)	ACD-1LAJ1	TBD-P1	ACD-W1
1LA	+Y, Left	Redundant(B)	ACD-1LAJ2	TBD-P2	ACD-W2
1LB	+Y, Left	Prime(A)	ACD-1LBJ3	TBD-P3	ACD-W3
1LB	+Y, Left	Redundant(B)	ACD-1LBJ4	TBD-P4	ACD-W4
1RA	+Y, Right	Prime(A)	ACD-1RAJ5	TBD-P5	ACD-W5
1RA	+Y, Right	Redundant(B)	ACD-1RAJ6	TBD-P6	ACD-W6
1RB	+Y, Right	Prime(A)	ACD-1RBJ7	TBD-P7	ACD-W7
1RB	+Y, Right	Redundant(B)	ACD-1RBJ8	TBD-P8	ACD-W8
2LA	-X, Left	Prime(A)	ACD-2LAJ9	TBD-P9	ACD-W9
2LA	-X, Left	Redundant(B)	ACD-2LAJ10	TBD-P10	ACD-W10
2RB	-X, Right	Prime(A)	ACD-2RBJ11	TBD-P11	ACD-W11
2RB	-X, Right	Redundant(B)	ACD-2RBJ12	TBD-P12	ACD-W12
3LA	-Y, Left	Prime(A)	ACD-3LAJ13	TBD-P13	ACD-W13
3LA	-Y, Left	Redundant(B)	ACD-3LAJ14	TBD-P14	ACD-W14
3LB	-Y, Left	Prime(A)	ACD-3LBJ15	TBD-P15	ACD-W15
3LB	-Y, Left	Redundant(B)	ACD-3LBJ16	TBD-P16	ACD-W16
3RA	-Y, Right	Prime(A)	ACD-3RAJ17	TBD-P17	ACD-W17
3RA	-Y, Right	Redundant(B)	ACD-3RAJ18	TBD-P18	ACD-W18
3RB	-Y, Right	Prime(A)	ACD-3RBJ19	TBD-P19	ACD-W19
3RB	-Y, Right	Redundant(B)	ACD-3RBJ20	TBD-P20	ACD-W20
4LA	+X, Left	Prime(A)	ACD-4LAJ21	TBD-P21	ACD-W21
4LA	+X, Left	Redundant(B)	ACD-4LAJ22	TBD-P22	ACD-W22
4RB	+X, Right	Prime(A)	ACD-4RBJ23	TBD-P23	ACD-W23
4RB	+X, Right	Redundant(B)	ACD-4RBJ24	TBD-P24	ACD-W24

~~9.2.2.~~8.2.2. ACD Temperature Instrumentation and PDU

TBD

~~9.2.3.~~8.2.3. ACD Survival Temperature Instrumentation and Spacecraft

TBD

~~9.3.~~8.3. Signal Names

~~9.3.1.~~8.3.1. Signal Naming

The signal name format is: ACD_nnnnnn_##xy where

nnnnnn is the signal name
is an optional 2 digit number
x is A or B indicating the A or B interface
y is P or M indicating positive or negative for differential signals

All digital signals except ACD_CLK are transmitted and received low true and so indicated by using "N" as the first character of the signal name. This convention is used to take advantage of the fact that the LVDS receivers default to the high state if the inputs open or are disconnected.

~~9.3.2.~~8.3.2. Signal List

A list of each of the signal wires between the ACD and the AEM (A interface only) is detailed below in Table 3.

TABLE 3. Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_CLK_AP	Clock+ to ACD	1	79	I	24 AWG, TP
ACD_CLK_AM	Clock- to ACD		78		
ACD_NSCMD_AP	Command+ to ACD	2	77	I	24 AWG, TP
ACD_NSCMD_AM	Command- to ACD		76		
ACD_NRST_AP	Reset+ to ACD	3	75	I	24 AWG, TP
ACD_NRST_AM	Reset- to ACD		74		
ACD_NSDATA_AP	Data+ to AEM	4	73	O	24 AWG, TP
ACD_NSDATA_AM	Data- to AEM		72		
ACD_NVETO_00AP	Veto Ch 0 + to AEM	5	71	O	24 AWG, TP

TABLE 3. Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_NVETO_00M	Veto Ch 0 - to AEM		70		
ACD_NVETO_01AP	Veto Ch 1 + to AEM	6	69	O	24 AWG, TP
ACD_NVETO_01AM	Veto Ch 1 - to AEM		68		
ACD_NVETO_02AP	Veto Ch 2 + to AEM	7	67	O	24 AWG, TP
ACD_NVETO_02AM	Veto Ch 2 - to AEM		66		
ACD_NVETO_03AP	Veto Ch 3 + to AEM	8	65	O	24 AWG, TP
ACD_NVETO_03AM	Veto Ch 3 - to AEM		64		
ACD_NVETO_04AP	Veto Ch 4 + to AEM	9	63	O	24 AWG, TP
ACD_NVETO_04AM	Veto Ch 4 - to AEM		62		
ACD_NVETO_05AP	Veto Ch 5 + to AEM	10	61	O	24 AWG, TP
ACD_NVETO_05AM	Veto Ch 5 - to AEM		60		
ACD_NVETO_06AP	Veto Ch 6 + to AEM	11	59	O	24 AWG, TP
ACD_NVETO_06AM	Veto Ch 6 - to AEM		58		
ACD_NVETO_07AP	Veto Ch 7 + to AEM	12	57	O	24 AWG, TP
ACD_NVETO_07AM	Veto Ch 7 - to AEM		56		
ACD_NVETO_08AP	Veto Ch 8 + to AEM	13	55	O	24 AWG, TP
ACD_NVETO_08AM	Veto Ch 8 - to AEM		54		
ACD_NVETO_09AP	Veto Ch 9 + to AEM	14	53	O	24 AWG, TP
ACD_NVETO_09AM	Veto Ch 9 - to AEM		52		
ACD_NVETO_10AP	Veto Ch 10 + to AEM	15	51	O	24 AWG, TP
ACD_NVETO_10AM	Veto Ch 10 - to AEM		50		
ACD_NVETO_11AP	Veto Ch 11 + to AEM	16	49	O	24 AWG, TP
ACD_NVETO_11AM	Veto Ch 11 - to AEM		48		
ACD_NVETO_12AP	Veto Ch 12 + to AEM	17	47	O	24 AWG, TP
ACD_NVETO_12AM	Veto Ch 12 - to AEM		46		

TABLE 3. Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_NVETO_13AP	Veto Ch 13 + to AEM	18	45	O	24 AWG, TP
ACD_NVETO_13AM	Veto Ch 13 - to AEM		44		
ACD_NVETO_14AP	Veto Ch 14 + to AEM	19	43	O	24 AWG, TP
ACD_NVETO_14AM	Veto Ch 14 - to AEM		42		
ACD_NVETO_15AP	Veto Ch 15 + to AEM	20	41	O	24 AWG, TP
ACD_NVETO_15AM	Veto Ch 15 - to AEM		40		
ACD_NVETO_16AP	Veto Ch 16 + to AEM	21	17	O	24 AWG, TP
ACD_NVETO_16AM	Veto Ch 16 - to AEM		18		
ACD_NVETO_17AP	Veto Ch 17 + to AEM	22	19	O	24 AWG, TP
ACD_NVETO_17AM	Veto Ch 17 - to AEM		20		
ACD_NCNO_AP	CNO + to AEM	23	21	O	24 AWG, TP
ACD_NCNO_AM	CNO - to AEM		22		
ACD_HV_AP	High Voltage Monitor + to AEM	24	23	A	24 AWG, TP
ACD_HV_AM	High Voltage Monitor - to AEM		24		
ACD_TEMP_AP	Temp Monitor + to AEM	25	25	A	24 AWG, TP
ACD_TEMP_AM	Temp Monitor - to AEM		26		
ACD_VDD_0A	+3.3V Power to ACD	26	1	P	24 AWG, Twisted Wires
ACD_GND_0A	+3.3V Power Return		30		
ACD_VDD_1A	+3.3V Power to ACD		3	P	
ACD_GND_1A	+3.3V Power Return		31		
ACD_VDD_2A	+3.3V Power to ACD		4	P	
ACD_GND_2A	+3.3V Power Return		32		
ACD_28V_0A	+28V Power to ACD HVBS	27	5	P	24 AWG, Twisted Wires
ACD_28V_RTN_0A	+28V Return		33		
ACD_28V_1A	+28V Power to ACD HVBS		7	P	

TABLE 3. Signal List

Signal Name	Signal Description	Signal Bundle No.	Pin No.	Input (I) Output (O) Analog(A) Power (P)	Wire Type and Gauge
ACD_28V_RTN_1A	+28V Return		34		
Not Used	Pins 8-16, 27-29, 35-39 not used	28	rest	-	-

~~9.4.~~8.4. Digital Inputs and Outputs

LVDS is used for all digital signals. The signal current is 3.5 mA, and the termination resistor is 100 ohms.

~~9.5.~~8.5. Signal Description

ACD_CLK: 20 MHz ± 1% continuous, 45-55% duty cycle clock from the ACD Electronics Module (AEM).

ACD_NSCMD: The command signal from AEM. The ACD_NSCMD signal transitions on the trailing edge of ACD_CLK and is shifted into the ACD on the leading edge of ACD_CLK. A single start bit, (logic 1), signals the beginning of a command.

ACD_NRST: Reset from AEM. ACD_NRST is synchronous to ACD_CLK. ACD_NRST at logic one resets state machines and initializes registers and modes in ACD. The ACD_NRST is at least five ACD_CLK cycles.

ACD_NSDATA: Data from ACD. The ACD_NSDATA signal transitions on the leading edge of ACD_CLK. The beginning of a data packet indicated by a single start bit.

ACD_NCNO, ACD_NVETOs: Veto discriminator output signals from ACD. The ACD_NCNO interface signal is the OR of the selected (via command) HLD discriminators.

ACD_HV: Analog monitor of the high voltage power supply voltage output. 0 - 2.5 volts indicates 0 - full-scale volts at the supply output. Pseudo differential analog, with signal on ACD_HVP and ground on ACD_HVN, 10K ± 5% source impedance all lines.

ACD_TEMP: ACD board temperature monitor, 30K thermistor, GSFC S-311-P-18 series (YSI 44900 series).

ACD_VDD(0-2): +3.3V supplied by the AEM to the ACD FREE circuit cards.

ACD_28V(0-1): +28V supplied by the AEM to the ACD HVBSs.

~~9.6.~~8.6. Switching characteristics timing diagram – Events and VETOs.

Any particle that generates an electrical signal above the VETO's threshold shall also force the GAFE's comparator to output a signal whose pulse duration is equal to the time the electrical signal is above the comparator's threshold. Two types of VETO signals shall be generated from the GAFE's comparator output, a VETO_AEM and a VETO_HITMAP.

~~9.6.1.~~8.6.1. VETO_AEM Signal Timing Characteristics

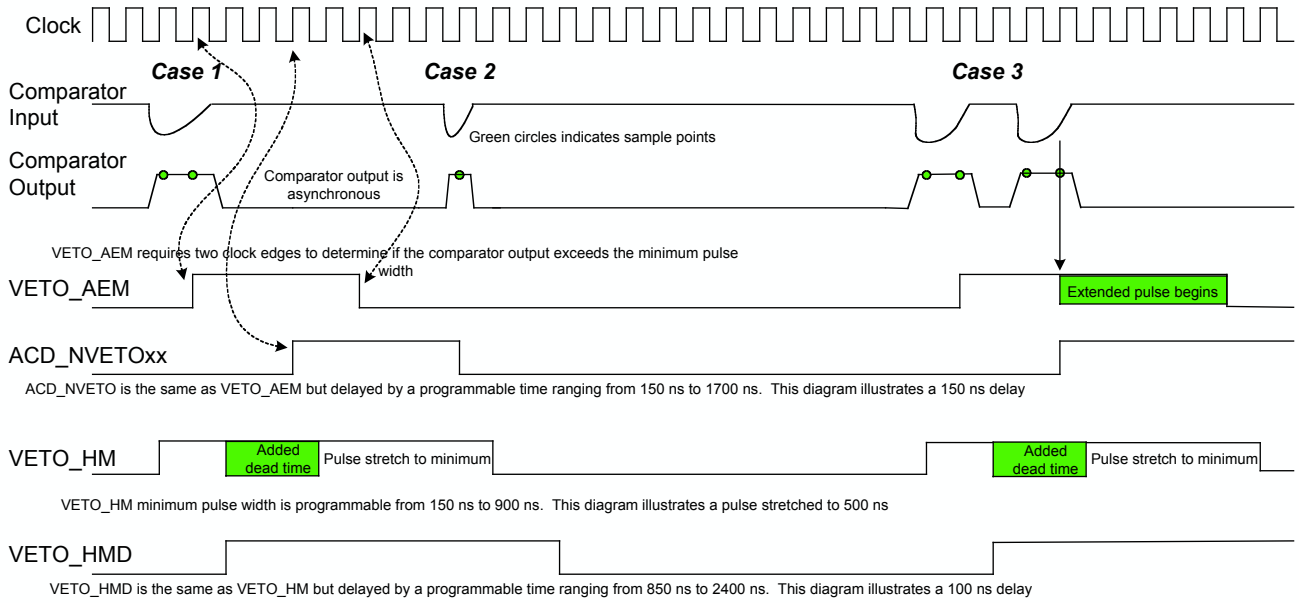
For generation of the VETO_AEM signals, the GARC shall contain digital delay lines, digital deglitch circuits and digital re-triggerable one shots. Each GAFE comparator output is first input to a digital delay line. A commandable delay tap (0 to 1550 nsec) is input to a deglitch circuit that looks for the delayed comparator signal to be present for at least two consecutive clock leading edges before a veto pulse is detected. Thus, the GARC will reject all input pulses of width less than 50 nsec, detect all input pulses of width greater than 100 nsec, and detect some and reject some pulses between 50 and 100 nsec in width. Once a pulse is detected, it fires a re-triggerable digital one-shot with width of 50 to 400 nsec (AEM commandable). The outputs of the one-shots are the ACD_NVETOxx signals. Note that for a minimum commanded delay of 0 nsec, the actual delay from discriminator input to ACD_NVETOxx output is 150 to 200 nsec (due to the synchronous circuitry) plus up to 20 nsec (due to I/O buffer and gate delays) in the GARC. For a maximum commanded delay of 1550 nsec, the actual delay from discriminator input to ACD_NVETOxx output is 1700 to 1750 nsec (due to the synchronous circuitry) plus up to 20 nsec (due to I/O buffer and gate delays) in the GARC.

~~9.6.2.~~8.6.2. VETO_HITMAP Signal Timing Characteristics

For generation of the VETO_HITMAP signals, the GARC uses the above delay lines with separate, commandable taps at 850 to 2400 ns. The delayed comparator pulse is stretched by 0 to 350 ns, commandable. The pulse is further stretched if necessary to meet a minimum pulse width of 150 to 900 ns, commandable. The final stretched pulse is sampled at trigger time, and read out in the event data as the hit map.

The following timing diagrams present what the VETO_AEM and VETO_HITMAP signals are for four different cases. The different cases are defined as follows:

Case 1: A charged particle event where the magnitude produces a comparator output that lasts at least 2 clock edges, but less than the VETO_AEM minimum pulse width.
Case 2: A charged particle event where the magnitude produces a comparator output that lasts less than 2 clock edges.
Case 3: Two charged particle events where each lasts at least 2 clock edges, but the second event occurs before the VETO_AEM pulse is complete.
Case 4: A charged particle event where the magnitude produces a comparator output greater than the VETO_AEM minimum pulse width.



The VETO_AEM signal is synchronized to the clock.

Figure 3. VETO Timing diagram (1)

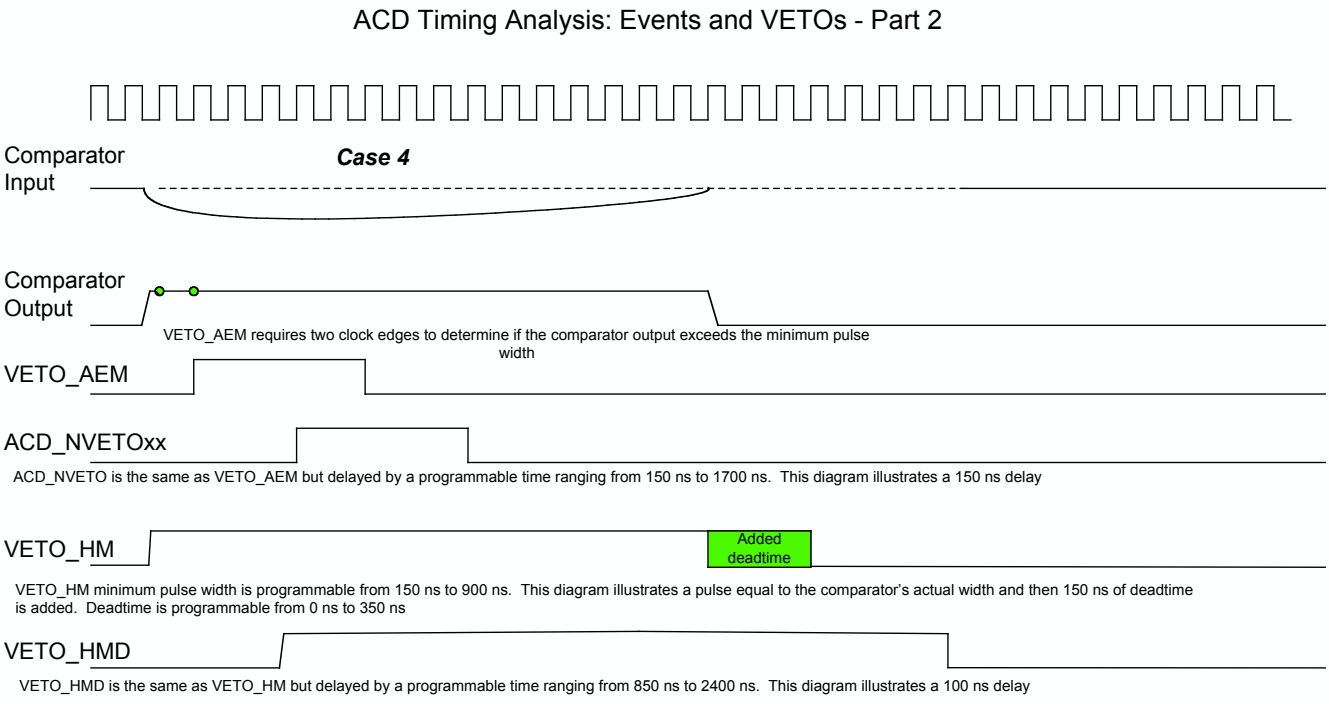


Figure 4. VETO Timing diagram (2)

~~9.7.~~8.7. Power

In each of the 24 cables, the ACD is supplied with +3.3 VDC nominal and +28 VDC nominal. All power uses redundant connector pins and wire in the cables (see table 2). Power to the ACD is supplied on both A and B AEM connectors. A and B AEM power will be wired together at each FREE board. The AEM will handle the power switching, protection, sensing and conditioning. All power requirements are specified at the BEA interface and are listed in the following paragraphs. The requirements on the power at the AEM interface are specified in LAT-SS-0183 Level IV Power Specification Document.

The noise on the 3.3 volt VDD shall be less than 5mV from DC to 1.0 MHz. The maximum peak noise shall be less than 5mV. The voltage shall be regulated to voltages between 3.2 and 3.6 volts.

The ACD_28V, ACD_28RTN supplies power for the PMT HVBS. The voltage spans +28 ± 1 V. The noise shall be less than 10 mV RMS from DC to 1.0 MHz. The maximum peak noise shall be less than 10 mV. The worst-case total consumption of the 12 HVBSs shall be less than 5.0 W at 38.7 V, maximum bus voltage. The nominal total consumption of the 12 HVBSs will be 2.4 W based on +28V bus voltage, 1 kV output and 30□A loading.

8.8. Grounding and Shielding

8.8.1. Grounding

The FREE circuit card is comprised of digital common, analog common, high voltage common and PMT common. All the commons are tied together on the FREE circuit card. See . The FREE circuit card's common point shall be grounded to the AEM via the common mode choke on the power return lines. The FREE analog circuitry shall be shielded in a Faraday shield that is connected to the common and isolated from the chassis ground. The grounding design shall make provisions to connect the commons to chassis ground at a later date, in case performance measurements yield the need for such a connection. The concern is that if the amplifier common is not connected to the shield, capacitive coupling from the front-end board shield (which is connected to the structure), will couple noise.

8.8.2. Shielding

The cable between the FREE circuit card and the BEA shall have a shield connected to chassis ground only on the BEA because the cable is expected to be less than 12 inches long. The cable between the BEA and the LAT EMI DAQ shall have the shields connected to chassis ground at the BEA and at the DAQ EMI.

8.9. EMI/EMC

The EMI/EMC performance is specified in GSFC-433-RQMT-005, the GLAST EMI/EMC Requirements Document. The maximum emission values allocated to the ACD sub-system are 14 dB (20%) of the maximum values specified in GSFC-433-RQMT-005.

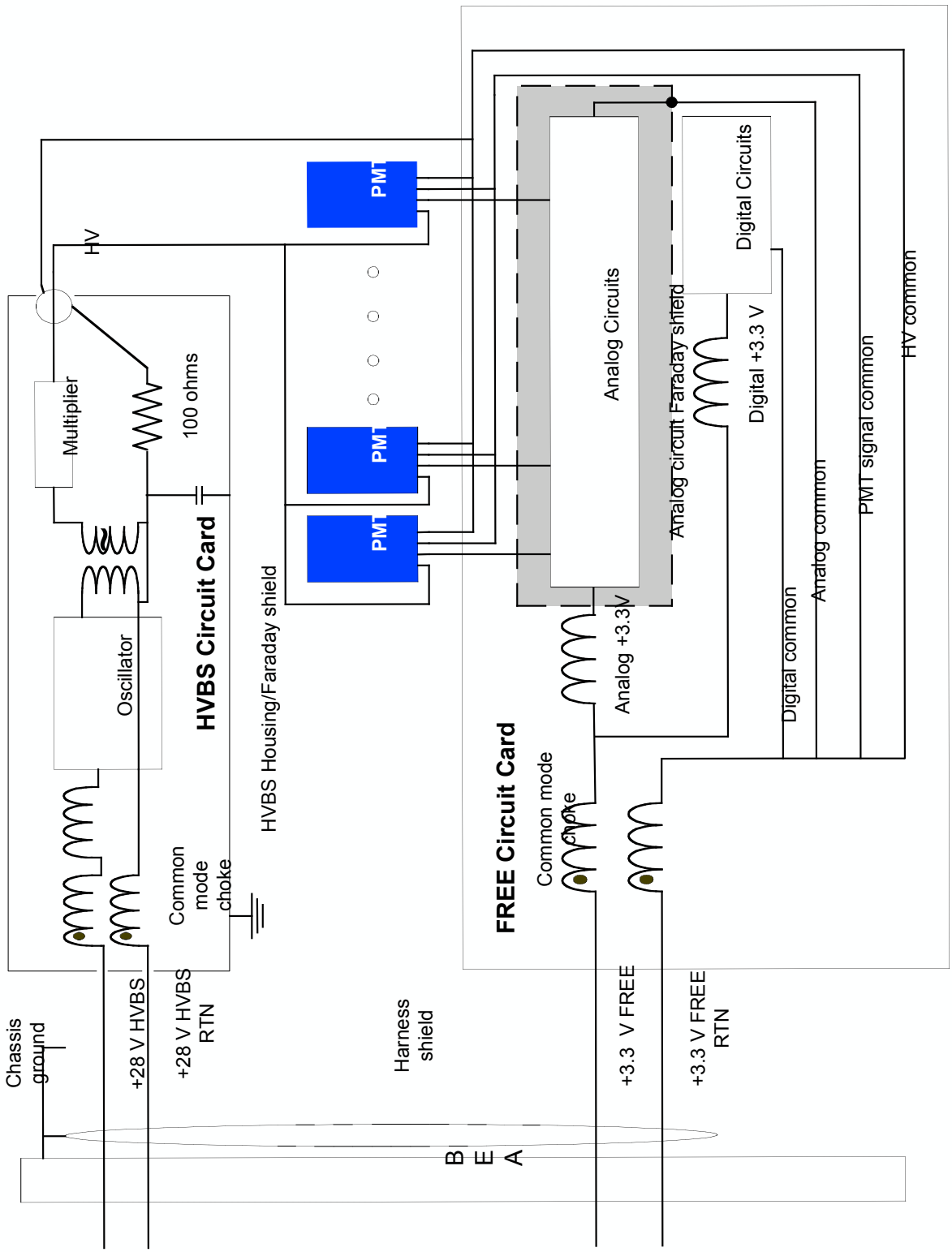


Figure 5. ACD Electronics Grounding

~~10.~~9. ACD Command and Data Format

All fields are MSB first (leftmost on drawings). Parity is odd. The data field is 16-bits. If a value of less than 16-bit is transferred from the AEM to the ACD, then the to-be-used bits are at the end of the field (leading zero's, the data is right justified). The same is true for data sent from the ACD to the AEM.

~~10.1.~~9.1. AEM to ACD Command Format

The AEM shall send either a trigger command or a configuration command to the ACD.

~~10.1.1.~~9.1.1. Trigger Command Format

Table 4: Trigger Command Format

Field	# Bits	Function
Start	1	1 for start
CMD Type Bits	2	10 to send only PHAs above threshold 01 to send all PHAs
CMD Type Parity	1	Odd Parity over previous 2 bits (without Start bit)

~~10.1.2.~~9.1.2. Configuration Command Format

Table 5: Configuration Command Format

Field	# Bits	Function
Start	1	1 for start
CMD Type	2	00 for command
CMD Type Parity	1	Odd Parity over previous 2 bits (without Start bit)
GAFE/GARC Select	1	0 for GARC 1 for GAFE
GAFE/GARC Address	5	GAFE: Select which GAFE, 0x1F for all GAFE GARC: Select which function block
Read/Write	1	0 for write, 1 for read
Data/Dataless	1	0 for dataless, 1 for data, always 1 for ACD
Register/function number	4	Which register/function in the function block
CMD Parity	1	Odd parity bit over previous 15 bits
Data	16	Data Field
Data Parity	1	Odd parity bit over previous 16 bits

Note: invalid command codes are decoded as no-ops

~~10.1.3.~~9.1.3. Command Protocol

The logic on the cable is low-true, so that a disconnected LVDS cable (asserts high) won't result in start bits.

Three types of commands may be sent to the ACD; trigger commands, write configuration commands, and read configuration commands.

The GARC does not execute a command if a parity error is detected. If there is a command error, then the command is copied to command error register. If there is only a data-field error, then the data field is copied to command error register. If both fields are in error, then only the command field is copied. In addition, the command and/or Data ERR bit is set. Error bits are reset when readout.

~~10.1.4.~~9.1.4. Command Processing Times

Command processing time is defined as the time from the leading ACD_CLK edge during the NSCMD start bit to the GARC being ready to accept another command start bit. The GARC test signal LIVE is used to measure this processing time. (The LIVE signal is only accessible at a

monitoring pin inside the FREE). Readback data to the AEM is sent towards the end of the processing time.

Table 6: Command Processing Times

Command Type	Processing time in nanoseconds
All GARC Write Configuration except as noted	2000
All GARC Read Configuration except as noted	3550
Cal Pulse	2000
Reset	2000
Set HVBS DAC	5400
Read HVBS DAC	7100
GAFE Configuration Write	12250
GAFE Configuration Read	13900

~~10.1.5.~~9.1.5. Trigger Processing

There are three phases of trigger processing.

The Trigger detect and ADC conversion phase starts with the leading edge of ADC_CLK during the TACK start bit and ends with "data_busy" (an internal GARC signal). This takes a minimum of 10950 ns. This time is extended by the amount that Hold_Delay exceeds 2750 ns. This time is also extended by the ADC_TACQ time.

detect_convert_time = 10950 + max(0 , (Hold_Delay – 2750)) + ADC_TACQ (ns)

The Count PHA phase takes 50 ns per PHA channel up to 900 ns. Minimum time is zero ns if Max_PHA is set to zero. The GARC counts PHAs starting with channel 0 until Max_PHAs (above threshold if in ZS mode) are found or channel 17 is reached.

The data transmission phase is from the NSDATA start bit to the end of PHA transmission. There are 39 fixed bits in the event data plus 0 to 18 15-bit PHA Words.

~~10.2.~~9.2. GAFE Registers

Table 7: GAFE Registers

Reg Number	Name	Values	Default State
0	CONFIG_REG	Bit 0: Test Charge Inject Gain, 0=low, 1=high	Low
		Bit 1: TCI Enable, 0=disable, 1=enable	Disable
		Bit 2: PHA Range Mode, 0=auto, 1=manual	Auto
		Bit 3: Range Select, 0=low, 1=high	LO
		Bit 4: Veto Discriminator Enable, 0=disable, 1=enable	Enable
		Bit 5: HLD Discriminator Enable, 0=disable, 1=enable	Enable
		Bits 15-6: Spare bits	0
1	VETO_DAC	0 – 63 3.2 to 0 nominal MIPs, steps of 0.05 MIPs	57➔0.35 (2)
2	HLD_DAC	0 – 63 64 to 0 nominal MIPs, steps of 1 MIP	38➔26
3	LLD_DAC	0 – 63 3.2 to 0 nominal MIPs, steps of 0.05 MIPs	55➔0.45
4	BIAS_DAC	0 – 63 1.75 to 2.2 V, steps of 56mV	32➔1.75 V
5	TCI_DAC	0 – 63 Test charge inject level	0
6	VERS_ADDR	Version Number, read only	
7	WRITE_CTR	Number of write commands since reset, read only	
8	REJECT_CTR	Number of command rejects since reset, read only	
9	LOOP_CTR	Number of commands since reset, read only	
10	CHIP_ADDR	GAFE Chip Address, read only	

Note 1: The GAFE Low Level Discriminator is not used by the FREE design. This signal was provided to zero-suppress PHA values. The PHA zero-suppress decision is instead done digitally in the GARC.

Note 2: The Default state format is: bits ➔ value

Note3: Reg 4, (BIAS_DAC) is a 6 bit register with a default of 32. Three ls bits are used by DAC.

~~10.3.~~9.3. GARC Registers

Table 8: GARC Registers

Function Block Address (5 bits)	Reg/Fct Number (4 bits)	Name	Description	Values	Initial State
0	1	Reset	Generates Reset for GARC registers and GAFE, write only	0	na
	2	Veto_Delay	Delay from Disc in to NVETO out	0-31 ➔ 150 - 1700, steps of 50 ns (see note 1)	5➔400 ns
	3	Calib	Set strobe high. Strobe is reset after trigger and PHA readout. write only	0	na
	8	HVBS	Specify normal HV Level	0-4095➔range from 0 to 1500 V (see note 2)	0
	9	SAA	Specify SAA HV Level	0-4095➔ range from 0 to 1500 V (see note 2)	0
	10	Use HV Normal	Write Sets HV DAC to Normal Level, read shift register in DAC	0	na
	11	Use HV SAA	Write Sets HV DAC to SAA Level, read shift register in DAC	0	na
	12	Hold Delay	Set Delay from Trigger (Leading edge of NSCMD) to Hold	0-127➔250-6600, steps of 50 ns	28➔1650 ns
	13	Veto Width	Pulse width of NVETO	0-7➔50-400, steps of 50 ns	2➔150 ns
	14	Hitmap Width	Minimum pulse width of Hitmap Signals (GARC internal)	0-15➔150-900, steps of 50 ns	7➔500 ns
	15	Hitmap Deadtime	Time added to Hitmap signals	0-7➔0-350, steps of 50 ns	3➔150 ns
1	4	Look at Me	GARC will enable this interface, A or B, write only	60304	
	8	Hitmap Delay	Delay from Disc in to Hitmap signals	0-31➔850-2400, steps of 50 ns (see note 1)	16➔1650 ns
	9	PHA EN0 Reg	PHA readout enable, bits 15-0➔ channels 15-0	Bit per channel	65535➔ All Enabled
	10	VETO EN0 Reg	VETO enable, channels 15-0	Bit per channel	65535➔ All Enabled
	11	HLD EN0 Reg	HLD enable, channels 15-0	Bit per channel	65535➔ All Enabled
	12	PHA EN1 Reg	PHA readout enable, bits 1-0➔ channels 17 and 16	Least significant two bits	3➔Both Enabled
	13	VETO EN1 Reg	VETO enable, channels 17 and 16	Least significant two bits	3➔Both Enabled
	14	HLD EN1 Reg	HLD enable, channels 17 and 16	Least significant two bits	3➔Both Enabled
	15	Max PHA	Maximum number of PHA values to send	0-18	4

Function Block Address (5 bits)	Reg/Fct Number (4 bits)	Name	Description	Values	Initial State
2	8	GARC Mode	Bit 0: Set parity for return data, 0=ODD (default), 1=EVEN Bit 1-3: HVBS A Enable, 000=Disabled (default), 111=Enabled Bits 4-6: HVBS B Enable, 000=Disabled (default), 111=Enabled Bit 7: Parity Select for GAFE Cmd, 0=ODD (default), 1=EVEN Bit 8: AEM A Veto outputs, 0=OFF, 1=ON (default) Bit 9: AEM B Veto outputs, 0=OFF, 1=ON (default) Bit 10:Control for the test pin mux (0 = HitMap_Test, 1 = live)		768
	9	GARC Status (read only)	Bit 0: Interface side, 0-A (default), 1-B Bit 1: HV Enable 1 (default OFF) Bit 2: HV Enable 2 (default OFF) Bit 3: Veto Enable A (default ON) Bit 4: Veto Enable B (default ON) Bit 5: ZS Status		24
	10	Command Reg	Command or data from last command error (read only)	16 bits	0
	11	GARC Diagnostic	Bit 15: parity_error Bit 14: cmd_parity_error Bit 13: data_parity_error Bit 12: cmd_error Bits 11-8: diag state loop counter Bits 7-0: valid command counter	16 bits, read only	
	12	Cmd Reject Counter	Number of Rejected Commands	8 bits, read only	0
	13	Free Board ID	Hardwired Board Serial Number	8 bits, read only	
	14	GARC Version	Version of GARC Chip	3 bits, read only	
3	8	PHA Threshold 0	PHA must exceed threshold unless send all PHAs type trigger Default of 1114 based on: baseline of 2 volts full scale of 0.2 volts baseline 0 nominal MIPS full scale 10 nominal MIPS threshold 1 nominal MIPS Inversion of PHA values done in GARC	0-4095	1114
	9	PHA Threshold 1		0-4095	1114
	10	PHA Threshold 2		0-4095	1114
	11	PHA Threshold 3		0-4095	1114
	12	PHA Threshold 4		0-4095	1114
	13	PHA Threshold 5		0-4095	1114
	14	PHA Threshold 6		0-4095	1114
4	8	PHA Threshold 7		0-4095	1114
	9	PHA Threshold 8		0-4095	1114
	10	PHA Threshold 9		0-4095	1114
	11	PHA Threshold 10		0-4095	1114
	12	PHA Threshold 11		0-4095	1114
	13	PHA Threshold 12		0-4095	1114
	14	PHA Threshold 13		0-4095	1114
5	8	PHA Threshold 14		0-4095	1114
	9	PHA Threshold 15		0-4095	1114
	10	PHA Threshold 16		0-4095	1114
	11	PHA Threshold 17		0-4095	1114
	12	ADC TACQ	ADC Acquisition Time, additional time from Hold to start of ADC clocks, see Trigger Timing	0-63 ➔ 0-3150 ns	0

Note 1: Add 0 to 50 ns because of the asynchronous nature of the Discriminator input signal and add up to 20 ns for various propagation delays.

Note 2: The exact range and calibration curve will be provided at a later time, after the HVBS's are built.

~~10.4.~~9.4. GARC Interface Details

The GARC selects the A or B interface based on which side sent the last look_at_me command. A and B LVDS drivers for signals transmitted from the FREE to the AEM can be turned on (3.5 mA drive) and "off" (0.5 mA drive) via command. The design, characterization, testing, layout and verification of all LVDS interface circuitry are a LAT DAQ subsystem responsibility and are provided to GSFC.

~~10.4.1.~~9.4.1. Flip-Flop Cells, Global Clocking

The GARC and GAFE use cells from the Tanner library for all flip flop functions including DFF, DFF preset, and DFF reset. The asynchronous preset and reset are used to establish initial state and configuration values to the GARC and GAFE at power on and reset times. All flip-flop clocking is via the Tanner global clocking network with a loading setting of 7. The Tanner global reset feature is also used. Additional SEU tolerance for the high voltage enable flip-flops is achieved via triple redundancy.

~~10.4.2.~~9.4.2. Tanner I/O Pads

Standard Tanner I/O pads will be used by the GARC, including buffered CMOS input, buffered CMOS output, power input, ground input, and unbuffered (for the LVDS and other analog functions).

~~10.5.~~9.5. ACD to AEM Data Format

The ACD shall provide data to the AEM upon receiving either a trigger command or a read configuration command.

~~10.5.1.~~9.5.1. Configuration Readback Data

The ACD shall respond to the AEM's read configuration command with readback data. The data shall consist of thirty-two bits.

Table 9: Configuration Readback Data

Field	# Bits	Function
Start	1	1 for start
GAFE/GARC Select	1	Copy of write command field (0 for GARC, 1 for GAFE)
GAFE/GARC Address	5	Copy of write command field (Select which GAFE)
Read/Write	1	1 for read
Data/Dataless	1	Always 1
Register/function number	4	Copy of write command field (which register/function in the function block)
CMD Parity	1	Odd parity bit over previous 12 bits
Data	16	Data, MSB first
CMD/DATA ERROR	1	Error in parity detected
Parity	1	Odd parity bit over previous 17 bits

The CMD/Data error bit is set if command or data parity error are detected by the ACD. The states of the error bits are returned with each read command. The error bits are reset when read out.

~~10.5.2.~~9.5.2. Event Data

The ACD shall send event data to the AEM upon receiving a trigger command from the AEM.

Table 10: Event Data

Field	# Bits	Function
Start Bit	1	1 for start
Hit Map Bits	18	Bits 17-0 for channels 0-17, bit set if hit in channel
Zero Suppression Bits	18	Bits 17-0 for channels 0-17, bit set if PHA above threshold
CMD/Data ERROR	1	Error in command parity detected
Header Parity	1	Odd parity bit over previous 37 bits
PHA Words (quantity 0-18) Order: Channel 0 to channel 17	15	Bit 14: 1 if another PHA word follows this one, 0 if this is last one Bit 13: 1 for high range, 0 for low range Bits 12-1: the PHA value, 0 to 4095 Bit 0: Odd parity over last 14 bits

The Hit Map bits indicate which channels had an active hit map signal at trigger time.

The ZS bits indicate which PHAs were above their threshold.

There are two trigger modes. On a normal_trigger, only PHAs above their threshold are sent. On a send_all_PHAs trigger, PHA values are sent regardless of their value. The number of PHAs sent is only up to Max_PHA.

Note that for PHA readout disabled channels, the ZS bits continue to function. Knowledge of the contents of the PHA_EN registers is needed to determine the channel numbers.

PHA_EN bits are used only for normal_trigger. PHAs are sent regardless of PHA_EN for send_all_PHAs trigger.

The condition of no PHA words sent can be detected by 15 zero bits after the Header Parity. Otherwise, at least one of the 15 bits will be set.

10.6.Grounding and Shielding

10.6.1.Grounding

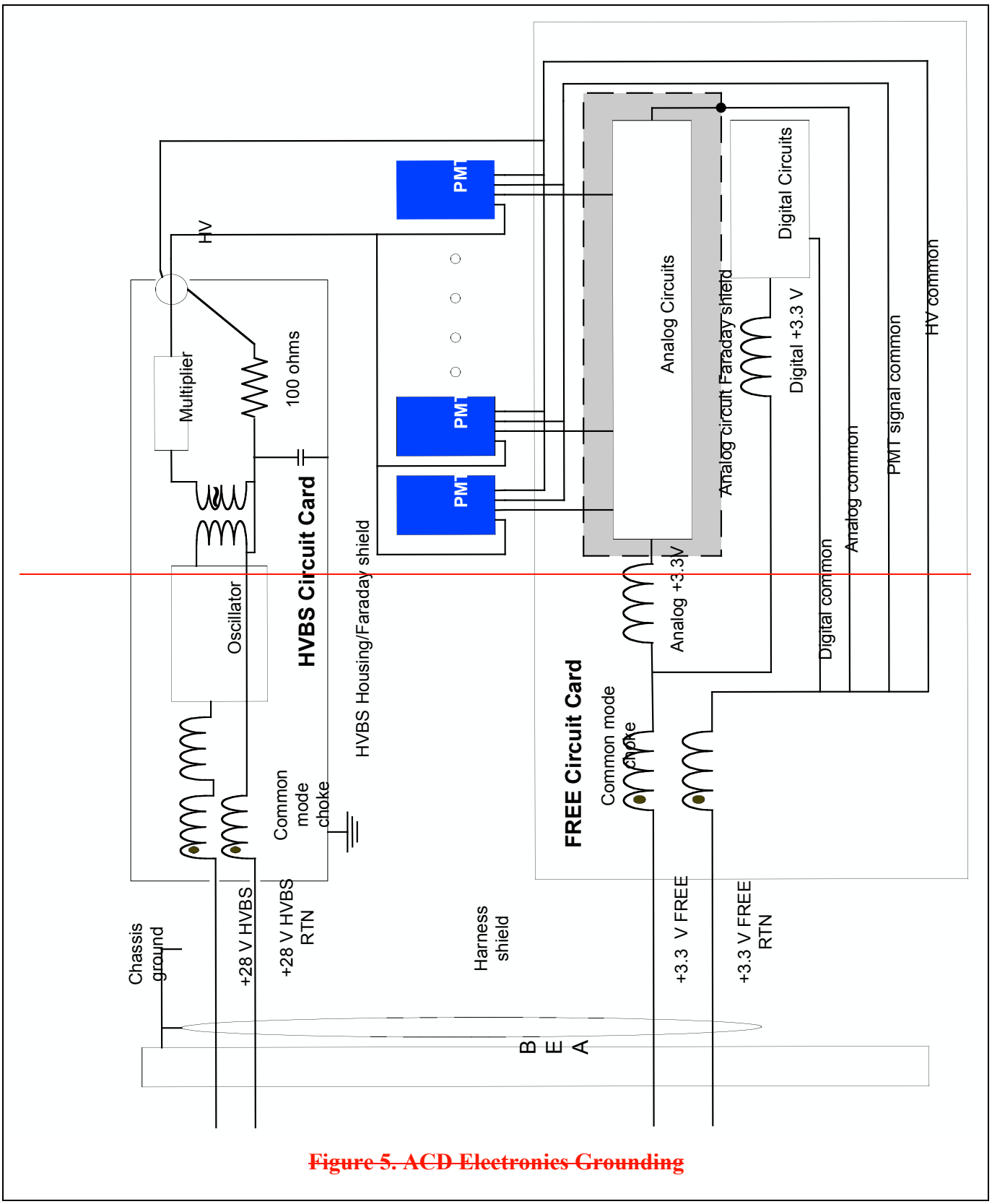
The FREE circuit card is comprised of digital common, analog common, high voltage common and PMT common. All the commons are tied together on the FREE circuit card. See Figure . The FREE circuit card's common point shall be grounded to the AEM via the common mode choke on the power return lines. The FREE analog circuitry shall be shielded in a Faraday shield that is connected to the common and isolated from the chassis ground. The grounding design shall make provisions to connect the commons to chassis ground at a later date, in case performance measurements yield the need for such a connection. The concern is that if the amplifier common is not connected to the shield, capacitive coupling from the front-end board shield (which is connected to the structure), will couple noise.

10.6.2.Shielding

The cable between the FREE circuit card and the BEA shall have a shield connected to chassis ground only on the BEA because the cable is expected to be less than 12 inches long. The cable between the BEA and the LAT EMI DAQ shall have the shields connected to chassis ground at the BEA and at the DAQ EMI.

10.7.EMI/EMC

The EMI/EMC performance is specified in GSFC-433-RQMT-005, the GLAST EMI/EMC Requirements Document. The maximum emission values allocated to the ACD sub-system are 14 dB (20%) of the maximum values specified in GSFC-433-RQMT-005.



~~Figure 5. ACD Electronics Grounding~~

~~11.~~10. Thermal Interface and Heat Transfer

~~12.~~The ACD has three thermal interfaces. First, the ACD-Grid interface is the primary means for conductive heat transfer. The second interface is the radiative thermal coupling to the outer space environment, through the MLI surrounding the ACD. The final interface is the radiative thermal interface between the ACD and the inside surface of the Tracker modules and Grid.

~~12.1.~~10.1. ACD Requirements

The maximum heat dissipated in the ACD during normal operating conditions shall be no greater than ~16 watts. The maximum orbit-average heat dissipated in the ACD during normal operating conditions shall be no greater than 11 watts.

The heat dissipation within the ACD shall be stable to within +/- 2 watts of the nominal during operations.

The bolted joint interface with the Grid shall be the primary mechanism for transferring heat into and out of the ACD.

The inside of the ACD and walls of the outer TKR modules are radiatively coupled. See current TKR thermal assumptions below.

The micrometeoroid/thermal shield covers the ACD per drawing LAT-DS-00309, LAT-ACD IDD. The ACD MLI shall have a maximum effective thru emissivity of 0.03 (TBR).

The LAT orbit altitude is a 450 Km, minimum, to 575 Km, maximum. The orbit inclination is 28.5 deg. The ACD shall use the on-orbit thermal environment heat flux values and SC thermal interface definitions as listed in the LAT-SC IRD, 433-IRD-0001.

For the purpose of LAT and ACD thermal analysis, the ACD shall be designed using the following thermal parameters:

- High emissivity(>.78), low alpha(<.2) on outer layer MLI blankets
- High emissivity(> .8) on BEA surfaces
- High Emissivity(>.8) on Shell face

Tracker Surface Property assumptions

- Black anodize or black paint with emissivity from .8 to .9

Grid Surface Property assumptions

- Black Anodize with emissivity BOL = 0.82, EOL = 0.78

Hot orbit scenario

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- The ACD hot-case orbit scenario is defined as identical to the LAT hot-case orbit. This is specified in LAT-TD-00224, "LAT Thermal Parameters."

Cold orbit scenario

- The ACD cold-case orbit scenario is defined as identical to the LAT cold-case orbit. This is specified in LAT-TD-00224, "LAT Thermal Parameters."

The exposure of the micrometeoroid/thermal shield to the SC solar panels is described in the LAT-SC IRD, 433-IRD-0001. The ACD does not view the LAT radiators.

Thermal testing of the ACD subsystem shall include at least 4 cycles in vacuum. ACD subsystem thermal tests and levels are listed in the ACD I&T plan.

Instrumentation (Thermocouples and thermistor) used for test are defined in LAT-TD-00890, LAT Instrumentation Plan and the LAT-TD-00430, ACD I&T Plan.

~~11.2.~~10.2. LAT Requirements

The temperature of the Grid side of the thermal interface with the Grid shall be kept within the limits shown in Table 11.

Table 11: Grid ACD interface temperature ranges.

State	Grid Int Tmin (degC)	Grid Int Tmax (degC)	Min TKR Temp (degC)	Max TKR Temp (degC)
Operating	-10 ~~degC~~	20 ~~degC~~	-10	25
Survival	-11.5 ~~degC~~	30 ~~degC~~	-20	-11.5
Ground Ops	TBD ~~degC~~	TBD ~~degC~~	N/A	N/A

Test temperatures for the ACD are captured in LAT-TD-00778, LAT Environmental Test Parameters.

~~12.~~11.Electrical Packaging Interfaces

~~12.1.~~11.1. Cable and Connector Definitions

The following list of cable will serve as the means for all electrical connection between the ACD and the LAT. Connector locations are shown on the ACD Outline Drawing, LAT-DS-TBD.

~~12.2.~~11.2. Cable Routing and Support (TBR)

Cable routing and cable support is detailed in the ACD Outline Drawing, LAT-DS-TBD.

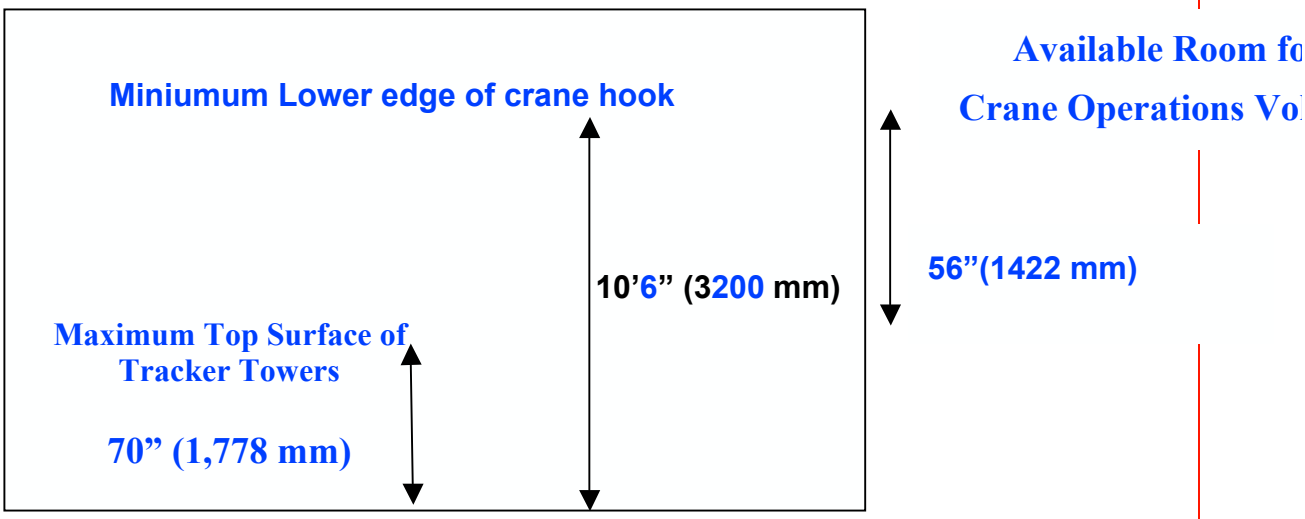
~~13.~~12. Integration and Test Interfaces

~~13.1.~~12.1. Integration Stay-Clears and Access Requirements

The ACD shall be integrated to the LAT vertically, from above.

The ACD shall be capable of being de-integrated from the Grid at any time. The de-integration of the ACD from the LAT will not require disassembly or invalidating verification of any other subsystem. Once the ACD is reintegrated, the only regression testing required is a limited electrical test to verify the ACD-LAT cable mates.

~~For integration of the ACD onto the LAT, the minimum distance from the top of the LAT TKR modules to the bottom of the crane lift point shall be greater than 1400 mm (TBR). (Note: a 25mm diameter attachment receptacle, centered over the ACD's X,Y center of gravity, can be accommodated.~~



~~**Figure 6. Vertical clearances in the LAT Integration Room -Refer to LAT-TD-00623**~~

The MLI micrometeoroid shield shall either be integrated after the ACD, or its bottom skirt shall be able to be folded up onto the ACD during and after integration, to provide access to the LAT region under the ACD stay-clear. However, as mentioned above, the MLI micrometeoroid shield currently ends at the bottom of the ACD BEA making this unnecessary in most instances.

The LAT will be supported at the Grid corners, with a frame that stays outside of the ACD useable envelope, as defined in LAT-DS-00309.

~~13.2.~~12.2. Provision for Surveying

During ACD integration, there shall be NO surveying lines-of-sight available from the top face of the Grid. The ACD shall not be capable of being aligned after integration on the Grid.

The surveying provisions are defined the LAT-MD-00895, LAT Instrument Surveying Plan. The ACD shall have a minimum of 4 surveying fiducials on the outside of Base Electronics Assembly, to allow its position to be surveyed after integration. These shall be at each of the 4 corners, with at least 3 visible at any time from a position off any corner of the LAT. ACD inner surfaces shall be surveyed with respect to these fiducials, so accurate information about the location of these surfaces will be available after the ACD has been integrated to the Grid.

~~Other ground Alignment Requirements - Fiducials on the ACD shall be surveyed to a precision of TBD mm, with respect to the LAT coordinate system.~~

~~13.3.~~12.3. Integration GSE

ACD lifting and integration fixtures shall not violate the ACD's useable envelope as defined in LAT-DS-00309. ACD lift interface zones with allowable force and moment vectors will be defined in LAT-DS-00309. During ACD integration, no GSE that would intrude in the ACD's usable envelope shall be mounted on top or on the sides of the Grid.
~~ACD lifting and integration fixtures shall not violate the ACD's useable envelope as defined in LAT-DS-00309.~~
~~ß~~The Multi Purpose Lift Sling used for ACD integration at GSFC will be difficult to use during LAT Integration due to height limitations. LAT I&T is responsible for the design, manufacture and proof test of the ~~and manufacturing of a separate~~ lift ~~sling~~ fixture for LAT-~~/~~ACD integration at SLAC. ~~Details of the attach points shall be given in LAT-DS-00309, as well as limiting force vectors and moments.~~

Note: Due to crane hook height limitations at the SLAC integration hall, it is not possible to use the Multi Purpose Lift Sling used for ACD integration at GSFC during LAT integration. For further clarification, details of the ACD sling used at GSFC are captured in the ACD Mechanical Ground Support Equipment document, ~~(~~ACD-REQ-7002~~). Any separate lift sling used on ACD should meet the following guidelines.~~

~~ßA stability analysis shall be performed in order to establish a positive margin of stability for the ACD and lifting apparatus.~~

~~ßThe lift sling attachments points to lift the ACD will be on the four corners of the BEA.~~

~~ßThe spreader apparatus (or any lift train hardware) shall, under operational loads, be at least 25 mm (~1") (TBR) from the uppermost surface of the ACD.~~

~~ßAny lift sling shall be proof tested as per NASA Technical Standard: *Standard for Lifting Devices and Equipment, NASA-STD-8719.96*. Proof load test factors: 2:1 initially; 1.25 (minimum):1 annually~~

~~ßLift sling should have a cover to prevent contamination due to oil or debris from the Hydra-Set or crane~~
~~ßLimiting force vectors and moments are detailed in LAT- DS-00309.~~.

12.3.1. ACD Responsibilities

12.3.1.1. MGSE

Development, fabrication, test, and delivery of the following mechanical ground support equipment (MGSE):

Lifting harnesses, shackles, and any other temporary hardware needed to support the ACD during integration on the LAT.

Handling Dolly to the support and move the ACD prior to integration to the LAT.

Any needed drill templates/pin templates.

Micrometeoroid shield/thermal blanket removal tools if needed.

ACD multi purpose test fixture.

Hydraset capable of manipulating ACD if needed.

~~13.3.1.2.~~12.3.1.2. EGSE

~~13.3.2.~~12.3.2. LAT Responsibilities

13.3.2.1 MGSE

Development, fabrication, and test of the following components:

Crane for lifting the ACD with its lifting fixture. Capacity->235 Kg.

Lifting fixture for the ACD to be used at SLAC. Design factor of safety shall be >3 times against minimum material yield strength.

13.3.2.2 EGSE

~~14.~~13. Other Interfaces

~~14.1.~~13.1. Venting

During launch, air from the ACD shall be vented outward, away from the inside of the LAT. No ACD venting shall be allowed into the volume surrounding the TKR modules or down past the Grid perimeter.

~~14.2.~~13.2. Particulates and Other Contamination~~.~~

The ACD shall contain all fracture-sensitive materials such that any particulates produced by a fracture are contained within the stay-clear volume of the ACD.

The ACD shall prevent any venting or shedding of particulates down, or out the bottom of its stay-clear, to avoid possible contamination of the spacecraft star tracker.

The ACD is sensitive to Helium and must be protected from concentrations greater than 5 parts per million, which is approximately the normal atmospheric concentration. Helium monitoring is required when the ACD is moved to a new location and then periodic monitoring thereafter.